WHAT IS CLAIMED IS:

1. A memory device for burn-in test, the memory device comprising:

an array of memory cells;

a plurality of word lines, each word line connected to a column of the array of memory cells; and

a leak-current limited unit connected to the array of memory cells via the plurality of word lines;

wherein during the burn-in test, the leak-current limited unit limits the current in each word line to a predetermined word line current value and a word line stress voltage is provided via the leak-current limited unit to stress each column of memory cells connected to one word line.

2. The memory device of claim 1, further comprising a plurality of bit lines, wherein each bit line is connected to a row of the array of memory cells, and wherein each memory cell comprises an access transistor and a storage capacitor, the gate of the access transistor is connected to one word line, the drain of the access transistor is connected to one bit line, and the source of the access transistor is connected to the storage capacitor.

3. The memory device of claim 1, wherein the leak-current limited unit further comprises:

a plurality of single word line leak-current limited units, wherein each single word line leak-current limited unit is connected to one word

line and limits the current in the word line to the predetermined word line current value.

4. The memory device of claim 3, wherein the single word line leak-current limited unit is a MOS transistor.

5. The memory device of claim 1, wherein the leak-current limited unit further comprises:

a plurality of sub-array word line leak-current limited units, wherein each sub-array word line leak-current limited unit is connected to a number of word lines and limits the total current flowing through the number of word lines to a predetermined sub-array current value.

6. The memory device of claim 5, wherein the sub-array word line leak-current limited unit comprises at least one level shifter, and each level shifter is used to limit current.

7. The memory device of claim 5, wherein the leak-current limited unit further comprises a plurality of single word line leak-current limited units, the sub-array word line leak-current limited units are connected to the word lines via the single word line leak-current limited units, and each single word line leak-current limited unit is connected to one word line and limits the current in the word line to the predetermined word line current value.

8. The memory device of claim 7, wherein the predetermined sub-array current value is between a first current value and a current value sum;

the first current value is a maximum current value which spare word lines are capable of supporting;

the current value sum is a sum of the first current value and a second current value; and

the second current value is the current value an additional spare word line is capable of supporting.

9. The memory device of claim 1, wherein the total current flowing into the memory device is limited to a predetermined total current, the predetermined total current is less than the maximum current value a voltage source is capable of providing, and the voltage source provides the word line stress voltage to the memory device.

10. A method for keeping the output of a word line driver in high impedance state during a burn-in test on a memory cell, wherein the word line driver has a cross-coupled load, the cross-coupled load comprising a first PMOS transistor and a second PMOS transistor, the source of the first PMOS transistor is connected to the source of the second PMOS transistor, the gate of the first PMOS transistor is connected to the drain of the second PMOS transistor, the gate of the second PMOS transistor is connected to the drain of the first PMOS transistor, and the output of the word line driver is located at the drain of the first PMOS transistor, the method comprising:

connecting the memory cell to the output of the word line driver through a word line;

keeping each MOS transistor, excluding the first PMOS transistor and the second PMOS transistor, at high impedance, wherein each MOS transistor is in the word line driver and is connected to the output of the word line driver;

applying a predetermined high voltage to the source of the first PMOS transistor so that both of the sources of the first PMOS transistor and the second PMOS transistor are kept at the predetermined high voltage; and

providing a predetermined low voltage to the output of the word line driver via a word line.

11. The method of claim 10, wherein the memory cell comprises an access transistor and a storage capacitor, the gate of the access transistor is connected to one word line, the drain of the access transistor is connected to a bit line, and the source of the access transistor is connected to the storage capacitor.

12. A switch circuit for switching between a normal data-in path and a burn-in test path in a burn-in test on a row of memory cells, the switch circuit comprising:

a data-in unit for sending input data to the row of memory cells via a bit line connected to the row of memory cells; and

a switch connected to the data-in unit for switching between the normal data-in path and the burn-in test path, the switch sending the input data selected from either the normal data-in path or the burn-in test path to the data-in unit; wherein

the switch circuit has a normal mode and a burn-in test mode;

in the normal mode, a read-write operation of the row of memory cells connected to the bit line is performed via the normal data-in path; and

in the burn-in test mode, a bit line stress voltage serves as the input data and is applied to the row of memory cells via the burn-in test path to perform the burn-in test.

13. The switch circuit of claim 12, wherein each memory cell comprises an access transistor and a storage capacitor, the gate of the access transistor is connected to a word line, the drain of the access transistor is connected to the bit line, and the source of the access transistor is connected to the storage capacitor.

14. A voltage generator for generating a substantially stable voltage, the voltage generator comprising:

a voltage dividing circuit for generating a first input voltage and a second input voltage according to a high reference voltage and a generator output voltage, wherein the high reference voltage is higher than the first input voltage, the first input voltage is higher than the

second input voltage, and the second input voltage is higher than the generator output voltage;

a first differential amplifier for generating a first output voltage signal in response to a reference input voltage and the first input voltage;

a second differential amplifier for generating a second output voltage signal in response to the reference input voltage and the second input voltage;

a first switch for providing a high voltage source to the generator output voltage when the first output voltage signal is at high state; and

a second switch for providing a low voltage source to the generator output voltage when the second output voltage signal is at high state; wherein

when the first input voltage is lower than the reference input voltage, the first output voltage signal is at high state so that the generator output voltage increases; and

when the second input voltage is higher than the reference input voltage, the second output voltage signal is at high state so that the generator output voltage decreases.

15. The voltage generator of claim 14, wherein the first switch is a MOS transistor and the second switch is a MOS transistor, the gate of the MOS transistor of the first switch is connected to the first output voltage signal, the drain of the MOS transistor of the first switch is connected to the high voltage source, the source of the MOS transistor of the first switch is connected to the drain of the MOS transistor of the second

switch, the gate of the MOS transistor of the second switch is connected to the second output voltage signal, the source of the MOS transistor of the second switch is connected to the low voltage source, and the drain of the MOS transistor of the second switch is connected to the generator output voltage.

16. The voltage generator of claim 15, further comprising:

a first mode switch circuit placed between the first differential amplifier and the first switch, the first mode switch circuit receiving a burn-in test mode signal; and

a second mode switch circuit placed between the second differential amplifier and the second switch, the second mode switch circuit receiving the burn-in test mode signal; wherein

when the burn-in test mode signal is enabled, the first mode switch circuit disconnects the first output voltage signal from the first switch and the second mode switch circuit disconnects the second output voltage signal from the second switch; and

when the burn-in test mode signal is disabled, the first mode switch circuit connects the first output voltage signal to the first switch and the second mode switch circuit connects the second output voltage signal to the second switch.

17. A memory device for a burn-in test, the memory device comprising:

a memory circuit, comprising:

an array of memory cells;

a plurality of word lines, each word line connected to a column of the array of memory cells; and

a plurality of bit lines, each bit line connected to a row of the array of memory cells;

wherein each memory cell is selected by one word line and one bit line;

a plurality of switch circuits, wherein each switch circuit is connected to one bit line, and each switch circuit switches between a normal data-in path and a burn-in test path in the burn-in test on a row of memory cells; and

a plurality of word line drivers, each word line driver comprising a cross-coupled load, each cross-coupled load comprising a first PMOS transistor and a second PMOS transistor, wherein the source of the first PMOS transistor is connected to the source of the second PMOS transistor, the gate of the first PMOS transistor is connected to the drain of the second PMOS transistor, the gate of the second PMOS transistor is connected to the drain of the first PMOS transistor, the output of the word line driver is located at the drain of the first PMOS transistor, and each word line driver is connected to one word line via the output of the word line driver.

18. The memory device of claim 17, wherein each memory cell comprises an access transistor and a storage capacitor, the gate of the access transistor is connected to one word line, the drain of the access

transistor is connected to one bit line, and the source of the access transistor is connected to the storage capacitor.

19. The memory device of claim 17, further comprising:

a leak-current limited unit connected to the array of memory cells via the plurality of word lines, wherein during the burn-in test, the leak-current limited unit limits the current in each word line to a predetermined word line current value and a word line stress voltage is provided via the leak-current limited unit to stress each column of memory cells connected to one word line.

20. A method for performing a burn-in test on a memory device of claim 17, the method comprising:

applying a predetermined high voltage to the sources of the first PMOS transistors of the word line drivers;

informing the memory device with a burn-in test mode signal;

applying a word line stress voltage to the word lines;

applying a cell plate voltage to the storage capacitors of the array of memory cells; and

applying a bit line stress voltage to the bit lines.

21. The method of claim 20, wherein when applying the bit line stress voltage to the bit lines, the cell plate voltage is alternately switched between a high state and a low state so that the voltage across a memory cell connected to a bit line and the voltage across the reference

memory cell connected to the complementary bit line is fully stressed by different voltage values.

22. The method of claim 21, wherein the data-in setup time and the data-in hold time is reserved at the rising edge and the falling edge of the alternately switching cell plate voltage.

23. The method of claim 20, wherein even word lines and odd word lines are grouped separately and the word line stress voltage is applied to the even word lines and to the odd word lines alternately.

24. The method of claim 23, wherein time needed for the word line transition delay is placed between the alternately switching word line stress voltage applied to the even word lines and the odd word lines.